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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/769,534	AKIYOSHI, HIDEO	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nc address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *07 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawing

The amendment and drawing correction submitted on Feb 7, 2002 have been reviewed and considered with the following results:

The proposed drawing correction has been approved, and the objection described in the previous Office Action has been withdrawn. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

The title change, and changes to the specification, have overcome all their respective objections described in the previous Office Action. Therefore, those objections have also been withdrawn.

Amended claims 2, 4, and 6 have overcome their rejections under 35 U.S.C. 112. These rejections have now been withdrawn. However, each of the amended claims now has its own minor objection, that is described later.

The amended claims did not overcome the prior art rejections of claims 1-7 as described in the previous Office Action. Those rejections include: 1) claims 1-7 under 35 U.S.C. 102(e) with respect to Malherbe; and 2) claims 1-3, 5, and 7 under 35 U.S.C. 102(e) with respect to Crotty. The basic rejections are repeated below, with some modifications to take into account the amended claim language. Comments, with respect to the applicant's arguments, are described under the Response to Arguments section.

Claim Objections

Claims 2, 4, and 6 are objected to because of the following informalities: To improve word flow, it is suggested --a-- be added prior to "corresponding" on line 4 in each of claims 2, 4, and 6. Appropriate corrections are required.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-7 remain rejected under 35 U.S.C. 102(e) as being anticipated by Malherbe, a reference cited in the previous Office Action's rejections. The invention of Malherbe provides a power-on reset means for an internal circuit (e.g. not shown but related to the disclosed "functional electronic circuit" on column 3, lines 56-65). In Fig. 3, Malherbe shows an integrated circuit comprising a sub reset signal generator CE1-CEn for generating a plurality of sub power-on reset signals POR1-PORn; and a main reset signal generator OR for generating a main power-on reset pulse signal POR that is used to initialize (related to the "an inhibiting means" disclosed on column 3, line 66 through column 4, line 15, and column 5, lines 7-10) the internal circuit according to the sub power-on reset signals POR1-PORn. It is understood that these signals include "at

least one from any of said sub power-on reset signals." One of ordinary skill in the art would know from Malherbe's disclosure that once the "inhibiting means" is deactivated, the internal circuit will be allowed to operate (e.g. turned on) because a sufficient power supply voltage is available for efficient operation. Fig. 4 shows details of each sub reset signal generator CE1-CEn. Since each generator has its own unique configuration, their respective sub power-on reset signal (i.e. POR1-PORn labeled in Fig. 3) will have a different timing than the other sub power-on reset signals, anticipating claim 1. Fig. 3 also shows a reset terminal (unlabeled) for receiving an external power-on reset signal TPOR, thus anticipating claims 3 and 5. Referring to Fig. 4, and interpreting the circuit differently, the sub reset signal generator is deemed the elements 10-13,20-23,30-34 which generate a plurality of sub power-on reset signals (e.g. the outputs of 12/13; 22/23; and 33/34) at different timings (due to the different configurations of the elements). The main reset signal generator comprises elements 15,16,24,33,36,OR for generating a main power-on reset signal POR in response to the sub power-on reset signals, thus anticipating claim 1 also. Since the main reset signal generator comprises a plurality of pulse generators (i.e. 15/16, 24, and 35/36) for generating pulses on the basis of a transition edge of a corresponding sub power-on reset signal, and a composite circuit OR for generating the main power-on reset signal POR, claim 2 is anticipated. [It is noted each pulse generator will generate a pulse in synch with a transition edge of a respective sub power-on reset signal. For example, when the rising edge of the voltage (sub power-on reset signal) from 12/13 reaches the switching threshold of inverter 15, pulse generator 15,16 will provide an associated transition

pulse.] Using the same type of reasoning as applied above, elements 50,51 of Fig. 5 are deemed a means for providing an external power-on reset signal to reset terminal - (of comparator 52), and comparator 52 can be deemed one of the plurality of pulse generators. Therefore, composite circuit OR generates the main power-on reset signal POR in response to the sub power-on reset signal(s) and external power-on reset signal, anticipating claims 4 and 6. When considering Figs. 3-5, one of ordinary skill in the art would recognize 15/16, 24, 35/36, and 52 generate a plurality of power-on reset pulse signals (i.e. POR1, POR2, PORn, and TPOR, respectively) according to a plurality of sub power-on reset signals (from 10-13, 20-23, 30-34, and 50/51, respectively), and OR initializes an internal circuit (not shown, but previously described above) by signal POR according to (at least one of) the power-on reset pulse signals. Therefore, claim 7 is also anticipated.

Claims 1-3, 5, and 7 also remain rejected under 35 U.S.C. 102(e) as being anticipated by Crotty, another reference cited in the previous Office Action's rejections. Crotty shows a circuit in Fig. 6 with blocks 630,640,650,210,220 closely corresponding to blocks 10,16,20,12,18, respectively of the applicant's own Fig. 1. [For example, Crotty's block 630 is shown in detail in Fig. 8(a). It is similar to the sub generator block 10 (12) of the applicant's Fig. 1 that is shown in detail in the applicant's Fig. 2, wherein both comprise a type of voltage divider/detector with its output being applied to at least one inverter. Examples of Crotty's blocks 220 and 650 are shown in Figs. 4(a) and 7, respectively. These blocks/details correspond to details of blocks 16 and 20 shown in the applicant's Fig. 1.] Fig. 6 shows a sub reset signal generator 630,210 for generating

a plurality of sub power-on reset signals VD2,VD1; and a main reset signal generator 640,220,650 for generating a main power-on reset pulse signal POR according to at least one of the sub power-on reset signals. Signal POR is used to initialize an internal circuit (not shown but disclosed as logic circuits or IC devices (e.g. see column 1, lines 6-31)). Since the configurations of circuits 630 and 210 are different from each other (e.g. see details of 630 in Fig. 8(a), and of 210 in Figs. 3(a) and 3(d)), their respective reset signals VD2 and VD1 will have different timings from each other, thus anticipating claim 1. The main reset signal generator 640,220,650 comprises a plurality of pulse generators 640,220 and a composite circuit 650. Each pulse generator 640,220 of Crotty could be configured as shown in Fig. 4(a), with details of the delay circuit 420 shown in Fig. 5(a). Deeming inverters 512-516 of Fig. 5(a) a delay in series with inverter 518, each pulse generator of Crotty corresponds to the pulse generators 16,18 shown in the applicant's own Fig. 1, wherein each pulse generator comprises a delay 22, inverter 24, and NAND gate 26. Fig. 7 of Crotty shows details of block 650. It comprises a NAND gate and inverter coupled in series, wherein the NAND gate receives the POR1,POR2 signals and generates signal POR. Therefore, claim 2 is also anticipated. Blocks 640,220 generate a plurality of power-on reset pulse signals POR2,POR1 according to a plurality of sub power-on reset signals VD2,VD1, and block 650 initializes an internal circuit (not shown, but previously described) according to at least one of the power-on reset signals POR2,POR1, anticipating claim 7. Fig. 10 of Crotty shows another embodiment of the circuit. This embodiment comprises a sub reset signal generator 630,210,930 for generating sub power-on reset signals

POR2,POR1; a reset terminal (not labeled) for receiving an external power-on reset signal POR3; and a main reset signal generator 1010 for generating a main power-on reset signal pulse POR. Therefore, applying the same type of reasoning as previously described (with respect to different timings, and the initialization of an internal circuit according to at least one reset signal), claims 3 and 5 are also anticipated.

No claim is allowable.

Response to Arguments

The applicant's arguments filed Feb 7, 2002 have been fully considered but they are not persuasive. The applicant argues: 1) the prior art fails to provide the advantages of the invention; 2) Malherbe discloses a neutralization device to block operation of any electronic circuit; 3) Malherbe doesn't disclose sub power-on reset signals at different timings; 4) neither Malherbe nor Crotty disclose a main power-on reset pulse signal to initialize an internal circuit; 5) Malherbe's OR circuit and Crotty's main reset signal generator don't output pulse signals; 6) Fig. 2 of Crotty doesn't disclose or suggest every element recited within the claims; 7) Crotty's circuit comprises two low pass filters; and 8) Crotty's circuit only detects noise. These arguments will now be addressed:

1) In response to the applicant's argument that the references fail to show certain features (e.g. advantages) of the applicant's invention, it is noted that the features upon which the applicant relies (i.e., "reliably generating a power-on reset signal") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also related to this

"fails to provide the advantages" argument, the applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

2-7) The applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. More specifically:

2) The applicant argues that Malherbe discloses a neutralization device to block operation of any electronic circuit. This is true with respect to the wording Malherbe cites within the patent. However, column 1, lines 23-52 of Malherbe discloses the relationship between known neutralization devices and power-on-reset control signal POR (that is clearly shown/used in the figures and disclosure) that one of ordinary skill in the art would recognize as a different means for describing a power-on reset circuit. For example, one of ordinary skill in the art would know that if a device is used to block operation of an electronic circuit, that device can also be used to allow the circuit to operate. Therefore, by considering the circuits and descriptions of Malherbe, one of ordinary skill in the art would recognize Malherbe's invention allows other circuits to operate only when the power supply voltage has reached a sufficient level for efficient operation. For example, see column 3, line 54 through column 4, line 10. Therefore,

without using a power-on reset circuit type label, Malherbe's neutralization device is clearly one type of a power-on reset circuit.

3) The applicant argues that Malherbe doesn't disclose sub power-on reset signals at different timings. However, as described in the prior art rejection, the configurations of each sub reset signal generator CE1-CE3 shown in Malherbe's Fig. 4 are different from one another. Therefore, one of ordinary skill in the art would know the timings of signals POR1-PORn (shown labeled in Fig. 3) will be different. Also, if the timings of signals POR1-PORn were not different, then each of them would transition at the same time, and thus only provide redundant signals to the OR gate. If that was the case, one of ordinary skill in the art would realize only one sub reset signal generator would be required to provide signal POR, and composite circuit OR would not be required to combine a number of identical signals.

4) The applicant argues that neither Malherbe nor Crotty disclose a main power-on reset pulse signal to initialize an internal circuit. Unless the examiner is mistaken, it is believed the main purpose of providing a power-on reset signal is for initializing the operation of some type of circuitry when a sufficient power supply voltage is available. Both Malherbe and Crotty provide a POR signal, and disclose the signal is used to either inhibit blocking the operation of a functional electronic circuit until the supply voltage is sufficient (e.g. Malherbe), or prevent logic circuits from functioning until after the supply voltage is adequate (e.g. Crotty). In both cases, one of ordinary skill in the art would know Malherbe's "functional electronic circuit" and Crotty's "logic circuits" are examples of internal circuits that would either be initialized to operate when the power

supply voltage reaches a sufficient level, or be prevented (i.e. inhibited or blocked) from operating if the power supply voltage is insufficient for efficient operation.

5) Related to the above argument, the applicant also argues that Malherbe's OR circuit and Crotty's main reset signal generator don't output pulse signals. Although only Figs. 1 and 2 of Malherbe show examples of POR pulses, one of ordinary skill in the art would know signal POR in Figs. 3 and 4 would be some type of a pulse signal. Also, since logic gate OR provides signal POR (as shown in Malherbe's Figs. 3 and 5), one of ordinary skill in the art would know signal POR is either a logic high or low (e.g. digital pulse). Crotty does not show a waveform for signal POR, but one of ordinary skill in the art would know it is also a pulse signal. For example, Crotty's buffer circuit 650 (shown as a block in Fig. 6, and in detail in Fig. 7) directly corresponds to composite circuit 20 shown in the applicant's own Figs. 1 and 4. Therefore, if the applicant's composite circuit (comprising a NAND gate and an inverter coupled in series) can provide a pulse signal POR, why wouldn't Crotty's Fig. 7 circuit do the same?

6) Pages 10 and 11 of the amendment appear to indicate that Fig. 2 of Crotty doesn't disclose or suggest every element recited within the claims. In this aspect, the examiner agrees entirely. However, why does the applicant concentrate on Fig. 2 when the rejection is clearly based on Crotty's other figures? After reviewing the previous Office Action's rejection, it is noted only Figs. 6, 8(a), 3(a), 3(d), 4(a), 5(a), 7, and 10 were clearly described. There was no mention of Crotty's Fig. 2 the applicant appears to concentrate on. However, the following two arguments are also related to Crotty's reference.

7) The applicant argues that Crotty's circuit comprises two low pass filters. If one goes specifically by labels, blocks 640 and 220 of Crotty's Fig. 6 are labeled as low pass filters and not pulse generators. However, when the entire disclosure is taken into account, details of a low pass filter are shown in Figs. 4(a) - 5(b). As described in the rejection, the low pass filter related to Figs. 4(a) and 5(a) correspond to blocks 16 and 18 of the applicant's own Fig. 1. For example, Crotty's low pass filter can comprise a NAND gate 410 and delay line 420 as shown in Fig. 4(a), wherein delay line 420 itself can comprise a delay 512-516 coupled in series with inverter 518 as shown in Fig. 5(a). Therefore, Crotty's low pass filter comprising NAND gate 410, delay 512-516, and inverter 518 correspond to the applicant's pulse generator NAND gate 26, delay 22, and inverter 24, respectively. Therefore, each of Crotty's low pass filters 640 and 220 (shown in Fig. 6) can also be deemed a pulse generator to correspond to the labeling used within the applicant's application.

8) The applicant also argues that Crotty's circuit only detects noise. This noise detection is only a part of one embodiment within Crotty's invention. However, Crotty clearly discloses the invention detects supply voltage failure and resets logic circuits. See column 2, lines 32-34. Although the embodiment comprising a low pass filter to detect noise is used to prevent spurious noise or ground bounces from causing resets (e.g. see column 3, lines 29-30), the main purpose of Crotty's invention is to provide a power-on reset signal if an inadequate supply voltage is detected (e.g. see column 3, lines 30-33).

Therefore, all the rejections described with respect to the references of Malherbe and Crotty in the previous Office Action, and also in this Office Action, are deemed proper to the understanding of one of ordinary skill in the art.

If the applicant still believes the references of Malherbe and Crotty still do not show/disclose all the claimed limitations (e.g. the internal circuit), it is noted that none of the applicant's own figures show main reset signal POR being applied to any type of circuit.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC

2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

17 April 2002

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